CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer comprising an organic material;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer.

2. The substrate of claim 1, wherein the integrated inductor comprises a spiral inductor.

3. The substrate of claim 1, wherein the integrated inductor comprises a microstrip loop inductor.

4. The substrate of claim 1, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

5. The substrate of claim 1, further comprising a second conductor layer fabricated on a lower surface of the first substrate layer, the second conductor layer adapted as a ground plane for the first conductor layer.

6. The substrate of claim 1, wherein the integrated inductor and the first conductor layer are configured in a coplanar waveguide arrangement.

7. The substrate of claim 1, wherein the integrated inductor comprises a cascaded loop inductor comprising one or more microstrip loop inductors cascaded together.

8. The substrate of claim 1, further comprising a second conductor layer fabricated on a lower surface of the first substrate layer, wherein two points of the integrated inductor are electrically connected through a via connected to the second conductor layer.

9. The substrate of claim 8, further comprising:

a second substrate layer fabricated on a lower surface of the second conductor layer; and

a third conductor layer fabricated on a lower surface of the second substrate layer.

10. The substrate of claim 9, wherein the second substrate layer comprises an organic material.

11. The substrate of claim 10, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

12. A method for fabricating a substrate adapted for use in integrated circuits, the method comprising the steps of:

fabricating a first substrate layer comprising an organic material;

fabricating a first conductor layer on an upper surface of the first substrate layer; and

fabricating an integrated inductor on an upper surface of the first conductor layer.

13. The method of claim 12, wherein the integrated inductor comprises a spiral inductor.

14. The method of claim 12, wherein the integrated inductor comprises a microstrip loop inductor.

15. The method of claim 12, wherein the organic material is at least one of an epoxy-based material, a liquid crystalline polymer, and a resin-coated polymer.

16. The method of claim 12, further comprising the step of fabricating a second conductor layer on a lower surface of the first substrate layer, the second conductor layer adapted as a ground plane for the first conductor layer.

17. The method of claim 12, wherein the steps of fabricating an integrated inductor and a first conductor layer comprise fabricating the integrated inductor as a coplanar waveguide inductor.

18. The method of claim 12, wherein the step of fabricating an integrated inductor further comprises cascading one or more microstrip loop inductors together.

19. The method of claim 12, further comprising the step of fabricating a second conductor layer on a lower surface of the first substrate layer, and wherein the step of fabricating an integrated inductor comprises electrically connecting two points of the integrated inductor through a via connected to the second conductor layer.

20. The method of claim 12, further comprising the steps of:

fabricating a second substrate layer on a lower surface of the second conductor layer; and

fabricating a third conductor layer on a lower surface of the second substrate layer.

21. The method of claim 20, wherein the second substrate layer comprises an organic material.

22. The method of claim 21, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

23. A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer, the integrated inductor comprising a microstrip spiral inductor having a strip width between approximately 4 mils and 40 mils and a line spacing between approximately 2 mils and 4 mils.

24. The substrate of claim 23, wherein the first substrate layer comprises an organic material.

25. The substrate of claim 24, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

26. The substrate of claim 23, wherein the line width, line spacing, and number of turns for the microstrip spiral inductor are configured to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

27. The substrate of claim 23, wherein the microstrip spiral inductor comprises a three-turn microstrip.

28. The substrate of claim 27, wherein the microstrip spiral inductor has a line width of approximately 10 mils, a line spacing of approximately 2 mils, and an area of approximately 4.4 millimeters^2.

29. The substrate of claim 28, wherein the microstrip spiral inductor has an effective inductance of approximately 12 nH at approximately 1.5 GHz, a maximum Q factor of approximately 80 at approximately 1.5 GHz, and a self resonating frequency of approximately 3.9 GHz.

30. The substrate of claim 27, wherein the microstrip spiral inductor has a line width of approximately 7 mils, a line spacing of approximately 2 mils, and an area of approximately 3.1 millimeters^2.

31. The substrate of claim 30, wherein the microstrip spiral inductor has an effective inductance of approximately 12 nH at approximately 1 GHz, a maximum Q factor of approximately 100 at approximately 1 GHz, and a self resonating frequency of approximately 3.2 GHz.

32. The substrate of claim 23, wherein the microstrip spiral inductor comprises a two-turn microstrip.

33. The substrate of claim 32, wherein the microstrip spiral inductor has a line width of approximately 10 mils, a line spacing of approximately 4 mils, and an area of approximately 3.2 millimeters^2.

34. The substrate of claim 33, wherein the microstrip spiral inductor has an effective inductance of approximately 7 nH at approximately 2 GHz, a maximum Q factor of approximately 100 at approximately 2 GHz, and a self resonating frequency of approximately 6.8 GHz.

35. The substrate of claim 32, wherein the microstrip spiral inductor has a line width of approximately 18 mils, a line spacing of approximately 4 mils, and an area of approximately 4.5 millimeters^2.

36. The substrate of claim 35, wherein the microstrip spiral inductor has an effective inductance of approximately 5.2 nH at approximately 2 GHz, a maximum Q factor of approximately 110 at approximately 2 GHz, and a self resonating frequency of approximately 7 GHz.

37. The substrate of claim 23, wherein the microstrip spiral inductor comprises a one-turn microstrip.

38. The substrate of claim 37, wherein the microstrip spiral inductor has a line width of approximately 34 mils, a line spacing of approximately 4 mils, and an area of approximately 3.2 millimeters^2.

39. The substrate of claim 38, wherein the microstrip spiral inductor has an effective inductance of approximately 1.5 nH at approximately 2.4 GHz, a maximum Q factor of approximately 170 at approximately 2.4 GHz, and a self resonating frequency of approximately 8.5 GHz.

40. A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer, the integrated inductor comprising a coplanar waveguide loop inductor.

41. The substrate of claim 40, wherein the first substrate layer comprises an organic material.

42. The substrate of claim 41, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

43. The substrate of claim 40, wherein the number of loops comprising the coplanar waveguide loop inductor is configured to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

44. The substrate of claim 40, wherein the coplanar waveguide loop inductor comprises hollow-ground coplanar waveguide loop inductor.

45. A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer, the integrated inductor comprising a microstrip loop inductor.

46. The substrate of claim 45, wherein the configuration of the microstrip loop inductor is designed to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

47. The substrate of claim 45, wherein the number of loops and the line width of the microstrip loop inductor are designed to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

48. The substrate of claim 45, wherein the microstrip loop inductor comprises a single loop having a line width of approximately 2 mils and an area of approximately 3.5 millimeters^2.

49. The substrate of claim 48, wherein the microstrip loop inductor has an effective inductance of approximately 7.7 nH, a maximum Q factor of approximately 90 at approximately 2.4 GHz, and a self resonating frequency of approximately 7.2 GHz.

50. The substrate of claim 45, wherein the microstrip loop inductor comprises two cascaded loops.

51. The substrate of claim 50, wherein the microstrip loop inductor has a line width of approximately 6 mils and an area of approximately 4.3 millimeters^2.

52. The substrate of claim 51, wherein the microstrip loop inductor has an effective inductance of approximately 7.8 nH, a maximum Q factor of approximately 110 at approximately 2.1 GHz, and a self resonating frequency of approximately 6 GHz.

53. The substrate of claim 52, wherein the microstrip loop inductor has a line width of approximately 4 mils and an area of approximately 3.5 millimeters^2.

54. The substrate of claim 50, wherein the microstrip loop inductor has an effective inductance of approximately 10.2 nH, a maximum Q factor of approximately 85 at approximately 2.2 GHz, and a self resonating frequency of approximately 5 GHz.

55. The substrate of claim 45, wherein the microstip loop inductor comprises three cascaded loops.

56. The substrate of claim 55, wherein the microstrip loop inductor has an area of approximately 4 millimeters^2 and a first portion of the microstrip loop inductor has a line width of approximately 4 mils and a second portion of the microstrip loop inductor has a line width of approximately 8 mils.

57. The substrate of claim 56, wherein the microstrip loop inductor has an effective inductance of approximately 15 nH, a maximum Q factor of approximately 80 at approximately 1 GHz, and a self resonating frequency of approximately 3.2 GHz.

58. The substrate of claim 55, wherein the microstrip loop inductor has an area of approximately 4 millimeters^2 and a first portion of the microstrip loop inductor has a line width of approximately 4 mils and a second portion of the microstrip loop inductor has a line width of approximately 2 mils.

59. The substrate of claim 58, wherein the microstrip loop inductor has an effective inductance of approximately 17 nH, a maximum Q factor of approximately 70 at approximately 1 GHz, and a self resonating frequency of approximately 3 GHz.

60. A method for fabricating a substrate having integrated components and adapted for use in integrated circuits, the method comprising the steps of:

fabricating a first substrate layer;

fabricating a first conductor layer on an upper surface of the first substrate layer; and

fabricating an integrated inductor on an upper surface of the first conductor layer, the integrated inductor comprising a microstrip spiral inductor having a strip width between approximately 4 mils and 40 mils and a line spacing between approximately 2 mils and 4 mils.

61. The method of claim 60 , wherein the first substrate layer comprises an organic material.

62. The method of claim 61, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

63. The method of claim 60, wherein the step of fabricating an integrated inductor further comprises configuring at least one of the line width, line spacing, and number of turns for the microstrip spiral inductor to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

64. The method of claim 60, wherein the microstrip spiral inductor comprises a three-turn microstrip.

65. The method of claim 64, wherein the microstrip spiral inductor has a line width of approximately 10 mils, a line spacing of approximately 2 mils, and an area of approximately 4.4 millimeters^2.

66. The method of claim 65, wherein the microstrip spiral inductor has an effective inductance of approximately 12 nH at approximately 1.5 GHz, a maximum Q factor of approximately 80 at approximately 1.5 GHz, and a self resonating frequency of approximately 3.9 GHz.

67. The method of claim 64, wherein the microstrip spiral inductor has a line width of approximately 7 mils, a line spacing of approximately 2 mils, and an area of approximately 3.1 millimeters^2.

68. The method of claim 67, wherein the microstrip spiral inductor has an effective inductance of approximately 12 nH at approximately 1 GHz, a maximum Q factor of approximately 100 at approximately 1 GHz, and a self resonating frequency of approximately 3.2 GHz.

69. The method of claim 60, wherein the microstrip spiral inductor comprises a two-turn microstrip.

70. The method of claim 68, wherein the microstrip spiral inductor has a line width of approximately 10 mils, a line spacing of approximately 4 mils, and an area of approximately 3.2 millimeters^2.

71. The method of claim 70, wherein the microstrip spiral inductor has an effective inductance of approximately 7 nH at approximately 2 GHz, a maximum Q factor of approximately 100 at approximately 2 GHz, and a self resonating frequency of approximately 6.8 GHz.

72. The method of claim 69, wherein the microstrip spiral inductor has a line width of approximately 18 mils, a line spacing of approximately 4 mils, and an area of approximately 4.5 millimeters^2.

73. The method of claim 72, wherein the microstrip spiral inductor has an effective inductance of approximately 5.2 nH at approximately 2 GHz, a maximum Q factor of approximately 110 at approximately 2 GHz, and a self resonating frequency of approximately 7 GHz.

74. The method of claim 60, wherein the microstrip spiral inductor comprises a one-turn microstrip.

75. The method of claim 74, wherein the microstrip spiral inductor has a line width of approximately 34 mils, a line spacing of approximately 4 mils, and an area of approximately 3.2 millimeters^2.

76. The method of claim 75, wherein the microstrip spiral inductor has an effective inductance of approximately 1.5 nH at approximately 2.4 GHz, a maximum Q factor of approximately 170 at approximately 2.4 GHz, and a self resonating frequency of approximately 8.5 GHz.

77. A method for fabricating a substrate having integrated components and adapted for use in integrated circuits, the method comprising the steps of:

fabricating a first substrate layer;

fabricating a first conductor layer on an upper surface of the first substrate layer; and

fabricating an integrated inductor on an upper surface of the first conductor layer, the integrated inductor comprising a coplanar waveguide loop inductor.

78. The method of claim 77, wherein the first substrate layer comprises an organic material.

79. The method of claim 78, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

80. The method of claim 77, wherein the step of fabricating an integrated inductor further comprises configuring the number of loops of the coplanar waveguide loop inductor to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

81. The method of claim 77, wherein the coplanar waveguide loop inductor comprises a hollows-ground coplanar waveguide loop inductor.

82. A method for fabricating a substrate having integrated components and adapted for use in integrated circuits, the method comprising the steps of:

fabricating a first substrate layer;

fabricating a first conductor layer on an upper surface of the first substrate layer; and

fabricating an integrated inductor on an upper surface of the first conductor layer, the integrated inductor comprising a microstrip loop inductor.

83. The method of claim 82, wherein the step of fabricating an integrated inductor further comprises configuring the microstrip loop inductor to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

84. The method of claim 82, wherein the step of fabricating an integrated inductor further comprises configuring at least one of the number of loops and the line width of the microstrip loop inductor to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

85. The method of claim 82, wherein the microstrip loop inductor comprises a single loop having a line width of approximately 2 mils and an area of approximately 3.5 millimeters^2.

86. The method of claim 85, wherein the microstrip loop inductor has an effective inductance of approximately 7.7 nH, a maximum Q factor of approximately 90 at approximately 2.4 GHz, and a self resonating frequency of approximately 7.2 GHz.

87. The method of claim 82, wherein the microstrip loop inductor comprises two cascaded loops.

88. The method of claim 87, wherein the microstrip loop inductor has a line width of approximately 6 mils and an area of approximately 4.3 millimeters^2.

89. The method of claim 88, wherein the microstrip loop inductor has an effective inductance of approximately 7.8 nH, a maximum Q factor of approximately 110 at approximately 2.1 GHz, and a self resonating frequency of approximately 6 GHz.

90. The method of claim 87, wherein the microstrip loop inductor has a line width of approximately 4 mils and an area of approximately 3.5 millimeters^2.

91. The method of claim 90, wherein the microstrip loop inductor has an effective inductance of approximately 10.2 nH, a maximum Q factor of approximately 85 at approximately 2.2 GHz, and a self resonating frequency of approximately 5 GHz.

92. The method of claim 82, wherein the microstip loop inductor comprises three cascaded loops.

93. The method of claim 92, wherein the microstrip loop inductor has an area of approximately 4 millimeters^2 and a first portion of the microstrip loop inductor has a line width of approximately 4 mils and a second portion of the microstrip loop inductor has a line width of approximately 8 mils.

94. The method of claim 93, wherein the microstrip loop inductor has an effective inductance of approximately 15 nH, a maximum Q factor of approximately 80 at approximately 1 GHz, and a self resonating frequency of approximately 3.2 GHz.

95. The method of claim 92, wherein the microstrip loop inductor has an area of approximately 4 millimeters^2 and a first portion of the microstrip loop inductor has a line width of approximately 4 mils and a second portion of the microstrip loop inductor has a line width of approximately 2 mils.

96. The method of claim 95, wherein the microstrip loop inductor has an effective inductance of approximately 17 nH, a maximum Q factor of approximately 70 at approximately 1 GHz, and a self resonating frequency of approximately 3 GHz.

97. A computer program embodied in a computer-readable medium for optimizing the design of an integrated inductor in a substrate adapted for use in integrated circuits, the computer program comprising:

logic configured to receive one or more design parameters for a substrate structure in which an inductor is to be integrated, the design parameters specifying at least one of the material characteristics, the physical characteristics, and electrical characteristics of one or more substrate layers and one or more conductor layers comprising the substrate structure;

logic configured to receive one or more process parameters associated with a predetermined type of integrated circuit package in which the substrate structure is to be implemented;

logic configured to generate a coupled-line model for a plurality of configurations for an integrated inductor, the coupled-line model comprising one or more coupled lines and one or more discontinuities;

logic configured to simulate the frequency response of the coupled-line models based on the design parameters and process parameters; and

logic configured to determine an optimal configuration for the integrated inductor which satisfies the design parameters and process parameters.

98. The computer program of claim 101, further comprising logic configured to provide the optimal layout for an integrated inductor.

99. The computer program of claim 97, wherein the logic configured to simulate the frequency response comprises:

segmenting the coupled-line model of the integrated inductor into individual segments;

calculating an impedance matrix for each of the segments in the coupled-line model; and

determining the frequency response of the combination of the segments.

100. The computer program of claim 99, wherein the logic configured to simulate the frequency response further comprises solving the following system of equations for each of a set of pairs of symmetric lossless coupled lines:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

wherein:

V_1 = voltage at a first node of a first lossless coupled line;
V_2 = voltage at a first node of a second lossless coupled line;
V_3 = voltage at a second node of the first lossless coupled line;
V_4 = voltage at a second node of the second lossless coupled line;
l = length of coupled lines;
Zoe = even-mode impedance;
Zoo = odd-mode impedance;
βe = even-mode propogation constant;
βo = odd-mode propogation constant;

$$\begin{aligned} Z_{11} = Z_{22} = Z_{33} = Z_{44} &= -j(Z_{oe}cot(\beta_e l) + Z_{oo}cot(\beta_o l))/2 \\ Z_{12} = Z_{21} = Z_{34} = Z_{43} &= -j(Z_{oe}cot(\beta_e l) - Z_{oo}cot(\beta_o l))/2 \\ Z_{13} = Z_{24} = Z_{31} = Z_{42} &= -j(Z_{oe}csc(\beta_e l) + Z_{oo}csc(\beta_o l))/2 \\ Z_{14} = Z_{23} = Z_{32} = Z_{41} &= -j(Z_{oe}cot(\beta_e l) - Z_{oo}csc(\beta_o l))/2 \end{aligned}.$$

101. The computer program of claim 97, wherein the logic configured to generate a coupled-line model is adapted to model at least one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

102. The computer program of claim 97, wherein the logic configured to receive one or more design parameters for a substrate structure is further configured to receive one or more design parameters for the integrated inductor to be designed.

103. The computer program of claim 102, wherein the one or more design parameters for the integrated inductor specifies a type of integrated inductor to be designed.

104. The computer program of claim 103, wherein the type of integrated inductor comprises one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

105. The computer program of claim 102, wherein the one or more design parameters for the integrated inductor comprises at least one of a predetermined line width for the integrated inductor, a predetermined line spacing for the integrated inductor, a predetermined maximum area for the integrated inductor, a predetermined inductance value for the integrated inductor, a predetermined frequency, a predetermined minimum Q factor for the integrated inductor, and a predetermined self resonant frequency for the integrated inductor.

106. A system for optimizing the design of an integrated inductor in a substrate adapted for use in integrated circuits, the system comprising:

means for receiving one or more design parameters for a substrate structure in which an inductor is to be integrated and one or more process parameters associated with a predetermined type of integrated circuit package in which the substrate structure is to be implemented, the design parameters specifying at least one of the material characteristics, the physical characteristics, and electrical characteristics of one or more substrate layers and one or more conductor layers comprising the substrate structure;

means for generating a coupled-line model for a plurality of configurations for an integrated inductor, the coupled-line model comprising one or more coupled lines and one or more discontinuities;

means for simulating the frequency response of the coupled-line models based on the design parameters and process parameters; and

means for determining an optimal configuration for the integrated inductor which satisfies the design parameters and process parameters.

107. The system of claim 106, further comprising a means for providing the optimal layout for an integrated inductor.

108. The system of claim 106, wherein means for simulating comprises:

means for segmenting the coupled-line model of the integrated inductor into individual segments;

means for calculating an impedance matrix for each of the segments in the coupled-line model; and

means for determining the frequency response of the combination of the segments.

109. The system of claim 108, wherein the means for simulating further comprises a means for solving the following system of equations for each of a set of pairs of symmetric lossless coupled lines:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

wherein:

V_1 = voltage at a first node of a first lossless coupled line;
V_2 = voltage at a first node of a second lossless coupled line;
V_3 = voltage at a second node of the first lossless coupled line;
V_4 = voltage at a second node of the second lossless coupled line;
l = length of coupled lines;
Zoe = even-mode impedance;
Zoo = odd-mode impedance;
βe = even-mode propogation constant;
βo = odd-mode propogation constant;

$$\begin{aligned} Z_{11} = Z_{22} = Z_{33} = Z_{44} &= -j(Z_{oe} cot(\beta_e l) + Z_{oo} cot(\beta_o l))/2 \\ Z_{12} = Z_{21} = Z_{34} = Z_{43} &= -j(Z_{oe} cot(\beta_e l) - Z_{oo} cot(\beta_o l))/2 \\ Z_{13} = Z_{24} = Z_{31} = Z_{42} &= -j(Z_{oe} csc(\beta_e l) + Z_{oo} csc(\beta_o l))/2 \\ Z_{14} = Z_{23} = Z_{32} = Z_{41} &= -j(Z_{oe} cot(\beta_e l) - Z_{oo} csc(\beta_o l))/2 \end{aligned}.$$

110. The system of claim 106, wherein the means for generating a coupled-line model is adapted to model at least one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

111. The system of claim 106, wherein the means for receiving further receives one or more design parameters for the integrated inductor to be designed.

112. The system of claim 106, wherein the one or more design parameters for the integrated inductor specify a type of integrated inductor to be designed.

113. The system of claim 112, wherein the type of integrated inductor comprises one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

114. The computer program of claim 111, wherein the one or more design parameters for the integrated inductor comprises at least one of a predetermined line width for the integrated inductor, a predetermined line spacing for the integrated inductor, a predetermined maximum area for the integrated inductor, a predetermined inductance value for the integrated inductor, a predetermined frequency, a predetermined minimum Q factor for the integrated inductor, and a predetermined self resonant frequency for the integrated inductor.

115. A system for optimizing the design of an integrated inductor in a substrate adapted for use in integrated circuits, the system comprising:

logic configured to receive one or more design parameters for a substrate structure in which an inductor is to be integrated, the design parameters specifying at least one of the material characteristics, the physical characteristics, and electrical characteristics of one or more substrate layers and one or more conductor layers comprising the substrate structure;

logic configured to receive one or more process parameters associated with a predetermined type of integrated circuit package in which the substrate structure is to be implemented;

logic configured to generate a coupled-line model for a plurality of configurations for an integrated inductor, the coupled-line model comprising one or more coupled lines and one or more discontinuities;

logic configured to simulate the frequency response of the coupled-line models based on the design parameters and process parameters;

logic configured to determine an optimal configuration for the integrated inductor which satisfies the design parameters and process parameters; and

a processing device configured to implement the logic.

116. The system of claim 115, further comprising a user interface device configured to enable a user to input the design parameters and the process parameters.

117. The system of claim 115, further comprising logic configured to provide the optimal layout for an integrated inductor.

118. The system of claim 117, further comprising a display device configured to display the optimal layout.

119. The system of claim 115, wherein the logic configured to simulate the frequency response comprises:

segmenting the coupled-line model of the integrated inductor into individual segments;

calculating an impedance matrix for each of the segments in the coupled-line model; and

determining the frequency response of the combination of the segments.

120. The system of claim 115, wherein the logic configured to simulate the frequency response further comprises solving the following system of equations for each of a set of pairs of symmetric lossless coupled lines:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

wherein:

V_1	=	voltage at a first node of a first lossless coupled line;
V_2	=	voltage at a first node of a second lossless coupled line;
V_3	=	voltage at a second node of the first lossless coupled line;
V_4	=	voltage at a second node of the second lossless coupled line;
l	=	length of coupled lines;
Zoe	=	even-mode impedance;
Zoo	=	odd-mode impedance;
βe	=	even-mode propogation constant;
βo	=	odd-mode propogation constant;

$$\begin{aligned} Z_{11} = Z_{22} = Z_{33} = Z_{44} &= -j(Z_{oe} cot(\beta_e l) + Z_{oo} cot(\beta_o l))/2 \\ Z_{12} = Z_{21} = Z_{34} = Z_{43} &= -j(Z_{oe} cot(\beta_e l) - Z_{oo} cot(\beta_o l))/2 \\ Z_{13} = Z_{24} = Z_{31} = Z_{42} &= -j(Z_{oe} csc(\beta_e l) + Z_{oo} csc(\beta_o l))/2 \\ Z_{14} = Z_{23} = Z_{32} = Z_{41} &= -j(Z_{oe} cot(\beta_e l) - Z_{oo} csc(\beta_o l))/2 \end{aligned}.$$

121. The system of claim 115, wherein the logic configured to generate a coupled-line model is adapted to model at least one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

122. The system of claim 115, wherein the logic configured to receive one or more design parameters for a substrate structure is further configured to receive one or more design parameters for the integrated inductor to be designed.

123. The system of claim 122, wherein the one or more design parameters for the integrated inductor specifies a type of integrated inductor to be designed.

124. The system of claim 123, wherein the type of integrated inductor comprises one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a microstrip spiral inductor.

125. The system of claim 122, wherein the one or more design parameters for the integrated inductor comprises at least one of a predetermined line width for the integrated inductor, a predetermined line spacing for the integrated inductor, a predetermined maximum area for the integrated inductor, a predetermined inductance value for the integrated inductor, a predetermined frequency, a predetermined minimum Q factor for the integrated inductor, and a predetermined self resonant frequency for the integrated inductor.